IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of Docket No. P27151

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Serial No:10/733,378 Group Art Unit: 2812

Filed: December 12, 2003 Examiner: Richard Booth

For: **STRAINED finFETS AND METHOD OF MANUFACTURE**

AMENDMENT

United States Patent and Trademark Office
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Alexandria, VA 22314

Sir :

Please amend the above-identified application as follows.

A listing of claims begins on page 2.

Remarks begin on page 9.

If extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to Deposit Account No. **09-0458**.

AMENDMENT TO THE CLAIMS

A copy of all pending claims and a status of the claims is provided below.

Claim 1. (original) A method of manufacturing a structure, comprising the steps of:

forming a first island of material having a first lattice constant;

forming a second island of material having a second lattice constant;

providing a mask over the first island and the second island which is used to form a tensile capping layer; and

forming at least a first finFET and a second finFET from the first island and the second island,

wherein the tensile capping layer prevents buckling one of the first and second finFET.

Claim 2. (original) The method of claim 1, wherein the first island is comprised of SiGe material and the second island is comprised of Si:C material and the mask is a nitride hard mask.

Claim 3. (original) The method of claim 1, wherein the first and second finFET are formed by sidewall image transfer and etching.

Claim 4. (original) The method of claim 1, further comprising selectively growing an Si epitaxial sidewall layer on sidewalls of the first finFET and the second finFET, wherein

the tensile capping layer prevents buckling of the at least second finFET during the growth of the Si epitaxial sidewall layer thereon.

Claim 5. (original) The method of claim 1, wherein:

etching forms the tensile capping layer from the hard mask on the first and second finFET;

the first finFET is comprised of SiGe and is placed in a tensile stress; and

the second finFET is comprised of is Si:C and is placed in a compressive stress.

Claim 6. (original) The method of claim 5, wherein the tensile capping layer prevents collapse or buckling of the Si:C finFET.

Claim 7. (original) The method of claim 1, further comprising:

forming shallow trench isolation (STI) in a substrate;

mixing the material into the substrate to form the first island and the second island by a thermal anneal process at a pFET region and a nFET region, respectively; and

wherein the STI relaxes and facilitates the relaxation of the first island and the second island.

Claim 8. (original) The method of claim 1, wherein the first island is formed by one of depositing and growing Ge material and the second island is formed by one of

depositing and growing Si:C or C material, the first island and the second island have a different relaxed crystal lattice.

Claim 9. (original) The method of claim 4, wherein the Si epitaxial sidewall layer has a different lattice constant than the first material and the second material such that the selectively grown Si epitaxial sidewall layer will strain tensilely and compressively on the first island and the second island, respectively.

Claim 10. (original) The method of claim 4, wherein the first finFET has a lattice constant a ≥ aSi and the second finFET has a lattice constant a ≤ aSi.

Claim 11. (original) The method of claim 1, wherein the first island is comprised substantially of SiGe and the second island is comprised substantially of Si:C and an epitaxially grown sidewall layer is grown on an etched SiGe finFET and Si:C finFET formed respectively from the SiGe island and the Si:C island, the SiGe finFET and the Si:C finFET is placed under a tensile stress and a compressive stress, respectively, by virtue of lattice matching of the epitaxially grown sidewall layer to the SiGe and Si:C finFET.

Claim 12. (original) A method of manufacturing a semiconductor structure, comprising the steps of:

forming shallow trench isolation (STI) in a substrate with a first material;

forming a first island associated with a pFET region and a second island associated with an nFET region;

providing a hard mask in tensile stress over the pFET region and the nFET region;

forming a pFET fin and an nFET fin with a capping layer of the hard mask in the pFET region and the nFET region, respectively; and

growing sidewalls on the pFET fin and the nFET fin, wherein the capping layer prevents buckling of the nFET fin during sidewall growth.

Claim 13. (original) The method of claim 12, wherein the pFET fin is made from a material comprised from SiGe and the nFET fin is made from a material comprised from one of Si:C or C.

Claim 14. (original) The method of claim 13, wherein the SiGe becomes tensilely strained and the Si:C becomes compressively strained and the hard mask prevents buckling of the nFET fin by substantially countering the compressive stress form by sidewall formation thereon.

Claim 15. (original) The method of claim 12, further comprising relaxing the STI and which facilitates relaxation of the first island and the second island during the thermally annealing step.

Claim 16. (original) The method of claim 12, wherein the sidewalls are comprised of Si which has a different lattice constant than the pFET fin and the nFET fin such that the Si sidewall will tensilely and compressively stress the pFET fin and the nFET fin, respectively.

Claims 17-20. (cancel)

Claim 21. (new) A method, comprising:

forming a structure comprising a shallow trench isolation (STI) between a first region and a second region;

depositing an epitaxial Ge material over a surface of structure;

providing an nFET hard mask on a portion of the Ge layer over the first region;

etching an exposed portion of the Ge layer;

stripping the nFET hard mask;

depositing a Si:C or C layer over the epitaxially deposited Ge material over the second region;

depositing a pFET hard mask on a portion of the Si:C or C layer on the first region;

etching exposed portions of the Si:C or C layer;

stripping the pFET mask; and

annealing the formed structure.

wherein during the annealing, for an nFET device, the deposited Ge layer is mixed into an underlying SOI film to form an island of substantially SiGe material and, for a pFET device, the deposited Si:C layer is mixed into the underlying SOI film forming an island of substantially Si:C material.

Claim 22. The method of claim 21, wherein the annealing takes place at about 1200°C to 1350°C between 1 hour and 10 hours.

Claim 23. (new) The method of claim 21, wherein the pFET hard mask is a nitride hard mask formed using spin-on coating, CVD, plasma-assisted CVD, ultrahigh vacuum chemical vapor deposition (UHVCVD), rapid thermal chemical vapor deposition (RTCVD), or limited reaction processing CVD (LRPCVD).

Claim 24. (new) The method of claim 21, wherein the depositing of the Si:C or C layer is by ultrahigh vacuum chemical vapor deposition (UHVCVD), rapid thermal chemical vapor deposition (RTCVD), or limited reaction processing CVD (LRPCVD) and other like processes.

Claim 25. (new) The method of claim 24, wherein a thickness of the Si:C or C material is between 5 to 50 nanometers.

Claim 26. (new) The method of claim 24, wherein the Ge layer has a percentage of Ge of less than 25% for the nFET device which does not cause defects in the structure.

Claim 27. (new) The method of claim 26, wherein, due to the annealing, the STI relaxes and facilitates the relaxation of the SiGe island and the Si:C island.

Claim 28. (new) The method of claim 21, wherein the SiGe island and the Si:C island have different relaxed crystal lattice which yield a substrate with small crystal islands.

Claim 29. (new) The method of claim 28, wherein the relaxation of the SiGe island and the Si:C island improves performance as compared to blanket (SiGe or Si:C) substrates.

Claim 30. (new) The method of claim 21, wherein the Ge layer is selectively etched using RIE, wet or dry etching.

REMARKS

Upon entry of this Amendment, claims 1-16 and 21-30 are currently pending in the application. Applicants request examination on the merits. Concurrently herewith Applicants are submitting a petition to withdraw from issuance, an RCE and an IDS with PTO-1449 form.

The Examiner is invited to contact the undersigned at the telephone number listed below, if needed.

Respectfully submitted,
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June 1, 2005
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